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PULSED POWER SYSTEM FOR THE HAPLS DIODE PUMPED LASER SYSTEM*

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Abstract

Industrial and Scientific High Energy Laser Systems with output energies in the Joule to Megajoule range typically rely on flash lamps to energize the gain media. Especially in rep rated laser systems the advantage of low capital cost per lamp is outweighed by many disadvantages, such as low pump efficiency, heating of the gain medium, frequent maintenance requirement, significant capital cost for its pulsed power system, and laser performance stability. Diode Pumped Solid State Laser (DPSSL) systems represent a viable alternative. In this paper we will present an efficient, integrated power conditioning system developed for the High-Repetition-Rate Advanced Petawatt Laser System (HAPLS) that is being developed by LLNL for deployment in the international user facility Extreme Light Infrastructure Beamlines (ELI-Beamlines) in Czech Republic [1].

The High Energy Pump Laser of HAPLS is energized by 4 High Peak Power Laser Diode Arrays with total peak power of 3.2 MW that were developed by Lasertel and LLNL. The diode arrays deliver ~1kJ at repetition rate 10Hz. Each diode array is comprised of 40 individual diode tiles where every tile generates >20 kilowatts of peak power.

Each tile is driven by a single pulser that contains its own energy storage, control and high current drive circuitry. As part of the HAPLS laser the pulsers are operated at approximately 520A, a pulse width of 300µs at 10Hz. In another LLNL laser system basically identical pulsers are operated at 315A, 300us at 120Hz.

The pulsers were designed to be operated in a support frame called a pulser crate. Each crate is designed to hold up to 45 pulsers in a volume similar to a desktop computer. Communication with the pulsers is by means of a one-way digital optical link which greatly simplifies the internal wiring. Each crate contains a "Brain Box" which in turn contains the front end processor (FEP), machine safety system (MSS) and energy storage dump subsystems.

Providing flexibility and system balancing capability each pulser can be tailored to the diode tile: it has an internal Arbitrary Waveform Generator (AWG) on board that controls the shape of the diode current pulse. The AWG can vary the pulse shape in any combination of programmable increments with resolutions 1A and 1µs up to maximums of 1kA and 350µs. Under command of the crate controller each pulser can create its own distinct waveform and deliver that waveform when triggered.

I. HAPLS LASER SYSTEM

HAPLS is being constructed at Lawrence Livermore National Laboratory in Livermore, California. The laser will be commissioned to an intermediary performance level before transport to ELI-Beamlines in Dolní Břežany, near Prague. Once at the facility HAPLS will be integrated in the ELI-Beamlines facility as one of four beamlines, and then ramped to its full performance. ELI-Beamlines is scheduled to begin operations in 2018.

Table 1. HAPLS design specifications.

Parameter	Value
Peak Optical Power	>1 PW
Energy per pulse short pulse	30 J
Pulse duration	30 fs
Pump laser energy	200 J
Repetition Rate	10 Hz
Electrical power consumption	<150 kW

II. DIODE ARRAYS

The power conditioning system uses laser diodes in place of flash lamps to provide energy to the amplifier in the Pump Laser. The laser diode arrays are manufactured by Lasertel Tucson, Arizona. Four arrays each provide 800kW peak optical power (3.2 Megawatts in total) at a wavelength of 888nm. Each array consists of 40 20kW "tiles" that produces ≈2.5kW average power when driven at 10Hz. Each tile is driven by a single pulser. The pulsers in turn are housed in a "crate" which can house up to 45 pulsers.

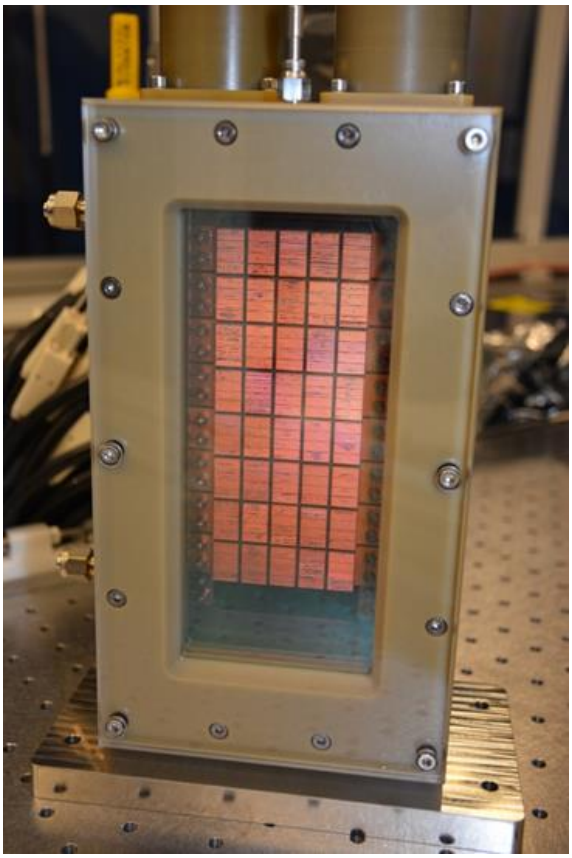

Figure 1 Laser Diode Array

III. PULSER

The pulsers provide drive current to the laser diode tiles. Each pulser is a compact unit 16.25"x 1.75"x1" (413 mm x 44.5 mm x 25.4 mm) weighing ≈2.5lbs (1.13 kg). As part of HAPLS the overall power conditioning system is the highest density (by volume) of any system in the world, by greater than an order of magnitude.

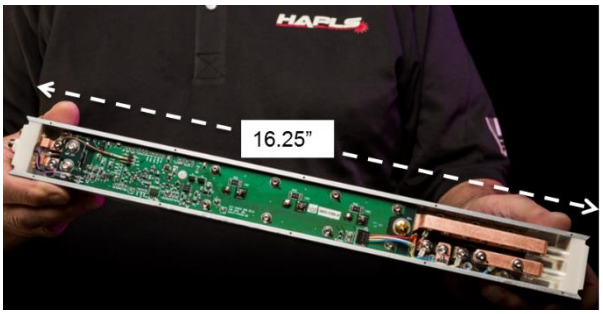

Figure 2 Pulser Assembly

Table 2. Pulser maximum operating parameters.

Parameter	Value	Comment
Peak current	1100 A	Dependent on load
Pulse Width	350 µs	Can be reprogramed for wider pulses
Repetition Rate	200 Hz	Dependent on cooling

As part of the HAPLS system a "crate" of 40 pulsers drives a single laser diode array.

Table 3. HAPLS operating point.

Parameter	Value	Comment
DC Operating Voltage	90 VDC	
Peak current	520 A	
Pulse Width	300 µs	
Repetition Rate	10 Hz	Tested at 20 Hz
Electrical power (pk)	50 kW	
Electrical Power (avg)	135 W	Per pulser
Electrical Efficiency	≈ 75 %	Energy delivered to laser diodes

Ten of the same pulsers (with a single resistor value change) are also used in the GOLD (Giga-Shot Optical Laser Demonstration) laser system at LLNL at a 120 Hz repletion rate. While the peak electrical power delivered is only approximately half that of HAPLS the average power per pulser is approximately 7.5 times greater.

Table 4. GOLD laser operating point.

Parameter	Value	Comment
DC Operating Voltage	82 VDC	
Peak current	315 A	
Pulse Width	300 µs	
Repetition Rate	120 Hz	
Electrical power (pk)	26 kW	
Electrical Power (avg)	1000 W	Per pulser
Electrical Efficiency	≈ 84 %	Energy delivered to laser diodes

The improvement in in electrical efficiency is due to the relatively higher impedance of the laser diodes in the GOLD system.

A. High Current Analog Drive Circuit

Figure 3 shows a simplified schematic diagram of the main high current portion of the diode pulsers. The main regulating components are two IXYS IXFK360N15T2 MosFETS. A 2mΩ current viewing resistor measures the current flowing in the FETs and the laser diode load, note that the laser diode load floats with respect to ground. The DC supply is isolated by a diode allowing many pulsers to be operated in parallel without the fear of a single pulser failure taking down the entire bank of pulsers. In like

manner the steering diode attached to the dump resistor line allows for the use of a single high energy dump system for an entire crate of pulsers. The analog drive signal to the op-amp is supplied by an Arbitrary Waveform Generator (AWG) that is discussed later.

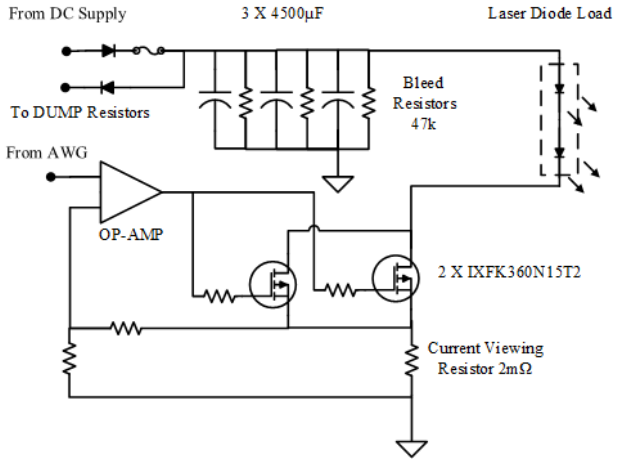

Figure 3. Simplified High Current Analog Circuit

B. Energy Storage Bank

Each pulser contains its own local energy storage capacitor bank consisting of 3 Evans Capacitor Company TDD3125452 4500µF/125WVDC tantalum "Hybrid" capacitors and their associated bleeder resistors. The capacitors deserve special note as they are a major enabling technology that reduces the volume of the capacitor bank by at least a factor of three while providing better ripple current characteristics and superior cooling compared to standard electrolytic devices. The use of these capacitors allows the incorporation of 100J of energy storage in approximately 3.5 cubic inches.

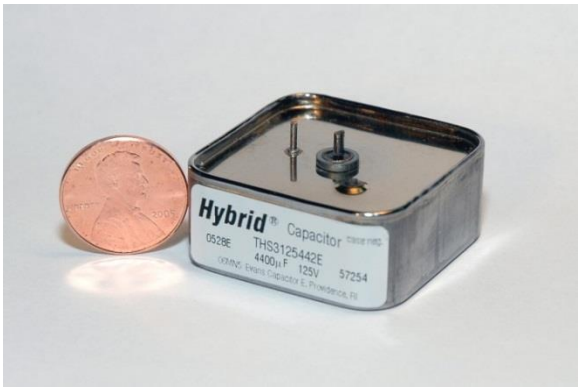

Figure 4 Energy Storage Capacitor

C. *Optical communications*

Each pulser has an internal microcontroller that controls its individual operation. A daughter board located under the main circuit board contains all the digital circuitry making up the controller. The microcontroller receives commands via a one way digital optical link from the crate. This link not only greatly simplifies the internal wiring of the crate but is also EMI resistant. The optical signal is transmitted by an array of 63 LED transmitters sending the same information. A unique digital address (based on serial number) is assigned to each pulser in much the same way that Ethernet system is configured. The link is highly reliable as that each pulser can "see" a minimum of 5 optical transmitters and the LEDs are driven by two redundant identical digital data streams. Under command of the crate controller each pulser can create its own distinct waveform and deliver that waveform when triggered.

D. *Arbitrary Waveform Generator*

The drive to each tile can be tailored individually to enable system balancing. The internal microcontroller also acts as an Arbitrary Waveform Generator (AWG) that controls the shape of the diode current pulse. The AWG can vary the pulse shape in any combination of increments with resolutions 1A and 1µs up to maximums of 1kA and 350µs. The output of the AWG feeds a Digital to Analog converter which in turn feeds a high current analog drive circuit described in section III A. This feature is primarily used to set the rise time, fall time, pulse amplitude and pulse width that will be delivered to the load. However the current pulse shape can take any form within these constraints. As an example, many laser diodes optical outputs tend to droop during the current pulse due to a reduction in conversion efficiency caused by heat. The AWG can compensate for this effect by adding a counter slope to the diode drive current.

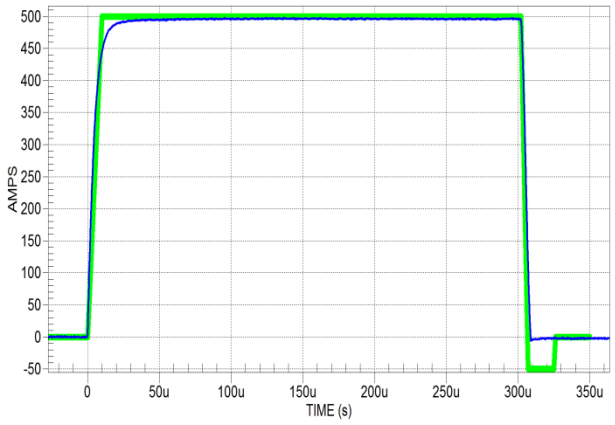

Figure 5 AWG Waypoints vs. Current

E. *Automated Pulser Testing*

~200 pulsers were manufactured by LLNL in support of the HAPLS and GOLD laser systems. To facilitate the testing of the pulsers before installation an automated test stand was constructed for quality assurance. The test stand is essentially a single pulser crate operating into a 100 milliohm / 200 watt resistor as a

surrogate for a laser diode tile. All aspects of pulser performance are tested including current amplitude, rise and fall times, pulse width and thermal performance. The test stand is capable of fully testing, calibrating and documenting a single pulser in approximately 15 minutes.

IV. PULSER CRATE

Pulsers are designed to be operated in a support structure called a pulser crate. The crate is designed to hold as few as one pulser and a maximum of 45 pulsers. The main crate is an aluminum assembly approximately the size of a large desktop computer. A picture of a pulser crate is shown in Figure 6. A crate provides the following services to each pulser:

* An optical data stream to control all pulsers (See Section III. C)
* Raw DC power
* Housekeeping power
* Energy dump system
* Pulser cooling
* Machine Safety System (MSS)

Figure 6 Pulser Crate and Optical Transmitter

A. *Pulser Cooling*

Each pulser is designed to reject all of its waste heat to the body of the pulser; therefore the individual pulsers must be mounted on a cold plate for extended operations. The crate provides 5 water cooled cold plates that are an integral part of the crate's mechanical structure. Figures 6 and 7 show the HAPLS configuration of 40 side mounted pulsers with the maximum of 5 pulsers on each face of the cooling plates. Up to 45 pulsers may be installed in this configuration (one side of one cold plate is reserved for the control electronics and the energy dump.) For higher power applications (such as GOLD) the pulsers must be mounted with their wide side against the cooling plate. Up to three pulsers may be mounted on each face of the cooling plates allowing for a maximum of 27 pulsers in this configuration.

A thermal interface material (TIM) is applied to the surface of the pulser that is in contact with the cold plate to facilitate heat transfer from the pulser body to the crate cold plates. The TIM used is a semi-flexible material that can be used and reused as crate configurations change.

V. BRAIN BOX

The brain box is an easily detachable sub-assembly of the pulser crate. In Figure 7 the brain box is located at the far left of the pulser crate. The sub-assembly contains the front end processor (FEP), machine safety system (MSS) and energy storage dump system..

A. *Front End processor (FEP)*

The FEP is responsible for handing communications with the upstream integrated control system, and control of the real time (RT) tasks required to operate the pulser crate.

B. FEP hardware

The FEP is implemented using National Instruments cRIO processors with an integrated FPGA and is programmed with National Instruments LabVIEW. The FEP communicates with the Integrated Control System (ICS) over Ethernet using the Asynchronous Message Communications (AMC) and Network Streams Communications protocols.

C. FEP Communications with ICS

The FEP receives configuration information from the ICS so that the diode arrays can be operated in a manner consistent with the current configuration of the laser as well as be consistent with other diode arrays in the overall system. The ICS can be as simple as a desktop computer running LabVIEW or as complex as the overall control system operating a multi-beam high energy laser.

D. FEP RT Tasks

The FEP is responsible for controlling all of the real time (RT) tasks required to operate the pulser crate. These tasks include control of the DC power supply used to provide raw power to the crate, generation of the bit stream used to control all pulsers, configuration of the machine safety system and monitoring of the overall crate environment.

The FEP creates the bit stream for pulser communications in accordance to the configuration information received from the ICS. The bit stream is then routed to the optical transmitter.

There are a number of environmental sensors within the crate that are monitored to ensure that all operations are within specified parameters. The FEP monitors these parameters and reports status back to the ICS for archiving and forensic information in the event of an off-nominal event.

E. Machine Safety System (MSS)

The MSS is implemented in the FPGA portion of the FEP and is responsible for shutting down operations in the event of an off-nominal event. All crate environmental monitors as well as a select set of diode array environmental monitors are digitized and evaluated at the trigger rate. All monitors are evaluated against set points that are provided by the ICS. When a set point exceeds the alarm limit pulser operations are stopped and a hardware line is activated that is monitored by the system MSS so that additional actions can be taken to protect the laser system. The monitor and control of the MSS is performed with the FPGA requiring no processor intervention with increases reliability and guarantees a deterministic response time.

Figure 7. Pulser Crate with 40 Pulsers

F. Trigger Generation

The FEP is responsible for generating the trigger signals for the pulsers in the crate. Triggers can be either internally generated or respond to external sources. The use of an external trigger allows for multiple pulser crates to be time synchronized. Internal triggers are mainly used for testing and are not synchronized to an external source.

G. Energy Storage Dump

The brain box also includes the dump system for all of the energy storage devices in the pulsers. By making the dump system common to all of the pulsers the overall volume required to implement the safety system is dramatically reduced without sacrificing performance or reliability. The dump system can be activated by an external personnel safety signal tied to an SIS system or by the internal MSS system which is also tied to the overall laser MSS system. Note that each energy storage capacitor has its own bleeder resistor to provide redundant protection.

H. Optical Communications

The crate includes an optical communication system used to transmit the digital data stream to each of the pulsers in the crate. Each pulser receives the optical communication and has a unique address so that it only acts upon commands meant for it. Pulsers also respond to a 'listen all' address. Using this method of communication each pulser can be individually programmed for current pulse shape but can be triggered simultaneously with all other pulsers in the crate. In Figure 6 the green PCB at the top is the optical transmitter assembly (See also section III. C)

VI. PULSER OUTPUT CABLES

In order to achieve high electrical efficiency and the desired pulse shape at the diode loads the cables used to deliver the current need to have as low a resistance and inductance as possible, be able to plug into both the pulser and the diode tile and be relatively easy to manufacture. The design of these cables meets those requirements with the following specifications:

Table 5 – Pulser Cable Parameters

Parameter	Value	Comment
Length	2 meters	Depends on load
Resistance	<1 mΩ / foot	
Inductance	< 10 nH / foot	
Pluggable	Yes	

Figure 8 is a picture of the completed cable assembly. Temp-Flex of South Grafton, Massachusetts supplied the custom coaxial cable with Litz-like wires sized to carry the required current (P/N TFC-495). The cable end connectors are an LLNL design that is simple to manufacture and install. Ends are keyed and polarized to prevent incorrect installation and diode tile damage.

Figure 8. Pulser Output Cables

VII. DC POWER SUPPLY AND SURGE SUPPRESSOR

Raw power for the pulser crate is provided by a COTS power supply that can be located as far away from

the crate as necessary (subject to IR losses). This allows the pulser to be close to the diode array to minimize cable length while reducing space requirements near the diode array. The voltage and current of the DC power supply is controlled by the crate FEP and communicates over optical Ethernet using TCP/IP protocol. Because the load on the power supply is pulsed we installed an inductive surge suppressor between the power supply and the crate to limit the load current transient that the power supply would be subjected to on each pulse. The surge suppressor is located in close proximity to the DC power supply and is configured for the operating characteristics of the system that it is installed in.

VIII. SUPERVISORY CONTROL

Because the pulser crate is designed to operate within a larger system it must communicate with that system's supervisory controls. This supervisory control system can be as simple as a PC with a user interface or as complex as a SCADA system running a power plant. In our case were connected to the HAPLS Integrated Control SYSTEM (ICS)

The supervisory control system provides the following services to the pulser crate:

* Pulser waveshape configurations
* MSS warning and alarm levels
* Trigger selection (internal or external)
* Trigger rate
* User Interface
* Data archiving

IX.SUMMARY

We have described the very compact, highly versatile power conditioning system of the HAPLS laser system in development at Lawrence Livermore National Laboratory. This technology is available for license and more information can be obtained by contacting the Industrial Partnerships Office at LLNL

X.REFERENCES

[1] https://www.llnl.gov/news/lawrence-livermore-build-advanced-laser-system-czech-republic

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